AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Figures 5 and 8. These sheets, which include Figures 5 and 8, replace the original sheet including Figures 5 and 8.

Attachment: Replacement Sheets (2)

REMARKS

Claims 1-3, 5-13, 15-33 and 35-37 are pending; claims 4, 14 and 32 having been cancelled. Applicant traverses the rejections set forth in the Office Action dated February 28, 2006.

PRIORITY DOCUMENTS

Applicant acknowledges and thanks the Examiner for the acknowledgement of priority under 35 U.S.C. §119, and further thank the Examiner for the acknowledgement of receipt of all of the necessary priority documents as shown in the Office Action dated February 28, 2006.

INFORMATION DISCLOSURE STATEMENT

Applicant acknowledges and thanks the Examiner for the careful consideration of all of the references listed in the Information Disclosure Statement filed May 12, 2005.

DRAWINGS

The Examiner has objected to FIGS. 5 and 8 for various typographical errors.

Applicant has amended FIGS. 5 and 8 to overcome the Examiner's objections.

OBJECTIONS TO THE SPECIFICATION

The Examiner has objected to the Specification for various typographical errors.

While Applicant generally agrees with the Examiner's objections and has amended the specification accordingly, Applicant traverses several of the objections.

With respect to page 13, paragraph [0036], line 6, Applicant submits that while the Specification refers to "DRA1k[0:X]." Figure 5 *incorrectly* refers to "DRA1y[0:X]." Applicant

has amended Figure 8 to correct for this typographical error. Accordingly, Applicant requests withdrawal of this objection.

With respect to page 16, paragraph [0043], Applicant submits that the specification correctly refers to "decoding signal DRA0k", as shown in FIG. 5.

With respect to page 19, paragraph [0048], lines 6-8, Applicant submits that no clarification is necessary. Lines 6-8 simply indicate that voltage passing from ND22 through MN24 will not affect MN27, assuming that current can flow through MN25 and MN26. This is due to the well-known understanding that current will always flow to ground when possible.

Accordingly, Applicant requests that the outstanding objections to the specification be withdrawn.

CLAIM OBJECTIONS

The Examiner objects to the use of two claims numbered "34". Applicant has re-enumerated claims 34-36 as claims 35-37. Accordingly, Applicant requests that these claim objections be withdrawn.

35 U.S.C. §112 CLAIM REJECTIONS

Claims 5, 6, 8-18, 21, 23-31, 34, 36 and 37 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which the Applicant regards as the invention. With respect to claim 5 and 8, both claims recite "an inverter coupled to a connection node of the second and third NMOS transistors, wherein the inverter drives a word line in the memory device." FIG. 3 illustrates an inverter INV connected to a node ND1. ND1 may also serve as a connection node of the second and third NMOS transistors which in the example embodiment may be among transistors 24 - 26.

Similarly, the embodiment of FIG. 7 also includes an inverter and multiple transistors connected through node ND22. The inverter may be comprised of MP24 and MN27 along with input voltage VPP and ground voltage VSS. The presence of an inverter is further supported by paragraph [0046].

With respect to claims 6 and 9, Applicant has amended the claims to overcome the Examiner's rejection.

With respect to claim 10, Applicant claims "a power terminal receiving a first high voltage that is higher than a power supply voltage of the device; a first transistor having a drain coupled to the power terminal, a source coupled to the first high voltage, and a gate coupled to a first input signal." One of ordinary skill in the art should readily understand that claim 10 recites a power terminal connected to a power supply voltage through a first transistor.

With respect to the use of the term "a second low voltage," Applicant has amended the claims to replace the phrase "first high voltage" and "second low voltage" with "high voltage" and "low voltage", respectively.

With respect to claim 15, Applicant submits that the arguments submitted with respect to claims 5 and 18 overcome the rejection of claim 15, as well.

With respect to claim 16, Applicant submits that "a voltage higher than the power supply voltage" need not be related to "the high voltage" recited in claim 10.

With respect to claim 21, Applicant has amended claim 21 to overcome the Examiner's rejection.

With respect to claim 25, Applicant submits that Fig. 4 is simply an example embodiment and should not be used to henceforth limit Applicant's claimed invention. Applicant is entitled to claim various embodiments within the spirit of the invention. Accordingly, Applicant submits that reciting "wherein the first NMOS transistor is controlled by a first input signal and the sixth

NMOS transistors controlled by an inverted version of the first input signal" is within the spirit of the invention. Accordingly, so long as the claims do not depart from the spirit of the invention, Applicant is not required to dictate claims following the precise specifications of each figure.

With respect to claim 30, Applicant has amended claim 30 to overcome the Examiner's rejection.

With respect to claim 31, Applicant submits that the arguments submitted with respect to claim 16, overcome the rejection of claim 31, as well.

With respect to claim 34, the subject matter of claims 34 has been incorporated into claim 32. Amended, independent claim 32 now recites "a third NMOS transistor operating at **one of the first voltage and second voltage** ...." Applicant submits that claim 32 sets forth in common, clear and standard language that the third NMOS transistor may operate at either one of a first voltage or a second voltage.

Accordingly, Applicant requests that the rejection of claims 5, 6, 8-18, 21, 23-31, 34, 36 and 37 under 35 U.S.C. §112 be withdrawn.

ALLOWABLE SUBJECT MATTER

Applicant acknowledges that claims 4, 7 and 27-28 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant acknowledges that claims 5, 6, 8, 9, 14-18 and 29-31 would be allowable if rewritten to overcome the rejections set forth under 35 U.S.C. §112, second paragraph. Applicant submits that independent claims 1, 10, and 32 have each been amended to incorporate the allowable subject matter of claims 4 or 14. Therefore, it is submitted that amended independent claims 1, 10, and 32 are allowable in view

of the Examiner's previous consideration of allowability of the subject matter added to these claims.

PRIOR ART REJECTIONS

35 U.S.C. §102(e) Hardee Rejection

Claims 1-3, 10-13 and 32-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Hardee (U.S. Patent No. 6,580,306). By this amendment, each of independent claims 1, 10, and 32 have each been amended to incorporate the allowable subject matter of claim 4 or 14. Accordingly, the rejection as to these claims and to those claims dependent thereon, is now moot.

35 U.S.C. §102(e) Wright Rejection

Claims 19-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Wright et al. (U.S. Patent No. 6,614,283). Applicant respectfully traverses this rejection.

FIG. 2 of Wright is directed to a voltage level shifter 200 which includes thin oxide N-MOS FET transistors 202 and 204, thick or medium oxide N-MOS FET transistors 206 and 208, thick oxide P-MOS FET transistors 210 and 212, and a thin oxide inverter 214. The digital input signal (V_{in}) 216 having a maximum voltage level set to be about the same as an internal operating voltage (V_{core}) 218, as the supplied to the voltage level shifter 200. The voltage level shifter uses digital input signal 216 to generate a digital output signal 220 having a maximum voltage level similar to that of an external transfer, or input/output (I/O) voltage (V_{IO}) 222.

With respect to claim 19, Applicant submits that Wright fails to teach, suggest, or render obvious, "a third MOS transistor coupled between the first internal node and the third internal node, and **having a relatively thin-gate insulation layer**; a fourth MOS transistor coupled between the second internal node and a fourth internal node, **having a relatively thin-gate**

insulation layer". On the contrary, Wright only teaches that N-MOS FET transistors 206 and 208 have thick or medium oxide layers.

The Examiner asserts that "third/fourth N-MOS transistors 206/208 can have a medium gate oxide (e.g., See Col. 4, lines 4-27). Since transistors with a medium-gate oxide have relatively thin gate insulation layers with respect to those transistors with a thick-gate oxide, claim 20 is anticipated."

Applicant submits that the Examiner is introducing an obviousness-type rejection into a 35 U.S.C. §102(e) rejection, or in the alternative, the Examiner is attempting to enter an inherency argument into a 35 U.S.C. §102(e) rejection. It is respectfully submitted that the outstanding Office Action does not provide a rationale or evidence tending to show either obviousness or inherency for the statements included in the Office Action regarding the subject matter originally formerly found in claim 20, and now found in claim 19. Applicant notes that the insertion of inherency or obviousness in the 102(e) rejection implies that there is a difference between the prior art being applied and the instant claim. [1],[2] That difference **requires that the Examiner supply an additional reference**.

Accordingly, if the Examiner continues to allege that Wright inherently discloses the features of amended, independent claim 19, it is respectfully submitted that the Examiner must abide by precedent and provide a basis in fact and/or technical reasoning to reasonably support the inherency determination.

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[1] [A] retrospective view of inherency is not a substitute for some teaching or suggestion which supports a selection and use of various elements in the particularly claimed combination. In re: Newell, 13 USPQ 2d 1248, 125 (Fed. Cir. 1989).

[2] "[I]n relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter 1990).

Absent the production of the basis in fact and/or technical reasoning to support the inherency statements, the case law requires the withdrawal of this rejection.

Accordingly, Applicant submits that Wright fails to teach, suggest, or render obvious all of the features of amended, independent claim 19; and respectfully requests that the rejection of amended, independent claim 19 and dependent claims 20-26, under 35 U.S.C. §102(e), be withdrawn.

CONCLUSION

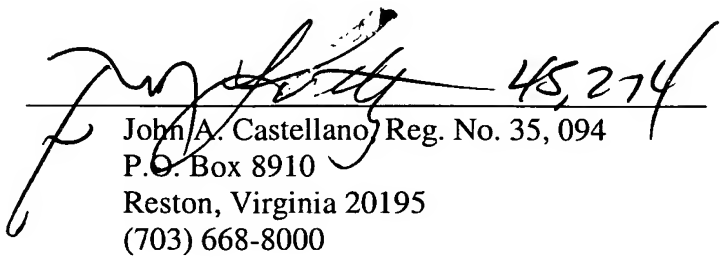
Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-3, 5-13, 15-33, and 35-37 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By  45,274

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